of a second transistor region in the semiconductor device substrate associated with a second transistor device in the semiconductor device to form [a] source/drain regions associated with the second transistor device with a channel region between said source/drain regions [using the first implantation process];

then forming a first gate oxide structure overlying a channel region in the first transistor region, the first gate oxide structure having a first thickness[;] and forming a second gate oxide structure overlying [a] the channel region in the second transistor region, the second gate oxide structure having a second thickness, the second thickness being greater than the first thickness.

Amend claim 2 as follows:

2. (Amended) The method of claim 1, further comprising the step of then implanting a portion of the first transistor region to form [a] source/drain regions associated with the first transistor device [using a second implantation process].

Amend claim 3 as follows:

3. (Amended) The method of claim 2, further comprising the steps of then[:] implanting a third transistor region associated with a third transistor device in the voltage associated with the third transistor device[;] and concurrently implanting a portion of a fourth transistor region in the semiconductor device substrate associated with a fourth transistor device in the semiconductor device to form [a] source/drain regions associated with the fourth transistor device with a channel region between said source/drain regions [using the third implantation process];

then forming a third gate oxide structure overlying a channel region in the third transistor region, the third gate oxide structure having a third thickness[;] and forming a fourth gate oxide structure overlying [a] the channel region in the fourth transistor region, the fourth gate oxide structure having a fourth thickness, the fourth thickness being greater than the third thickness.

Amend claim 4 as follows:

4. (Amended) The method of claim 3, further comprising the step of implanting a portion of the third transistor region to form a source/drain region associated with the third transistor device [using a fourth implantation process].

Amend claim 6 as follows:

6. (Amended) The method of claim 3, wherein the first and third transistor devices comprise NMOS transistors, wherein the second and fourth transistor devices comprise PMOS transistors, and wherein implanting the third transistor region and a portion of the fourth transistor region [using the third implantation process] comprises implanting phosphorus in the third transistor region and a portion of the fourth transistor region.

Amend claim 7 as follows:

7. (Amended) The method of claim 6, wherein implanting phosphorus in the third transistor region and a portion of the fourth transistor region comprises the steps of:

performing a phosphorus threshold adjustment implantation in the third transistor region and a portion of the fourth transistor region using a dose of about 8 E11 cm^{-2} and an energy of about 20 keV; and

performing a phosphorus punch-through implantation in the third transistor region and a portion of the fourth transistor region using a dose of about 2 E12 cm^{-2} and an energy of about 70 keV.

Amend claim 10 as follows:

10. (Amended) The method of claim 2, wherein the first transistor device comprises an NMOS transistor, wherein the second transistor device comprises a PMOS transistor, and wherein implanting a portion of the first transistor region [using the second implantation process] comprises implanting at least one of phosphorus and arsenic in a portion of the first transistor region.

Amend claim 12 as follows:

12. (Amended) The method of claim 1, wherein the first transistor device comprises an NMOS transistor, wherein the second transistor device comprises a PMOS transistor, and wherein implanting the first transistor region and a portion of the second transistor region [using the first implantation process] comprises implanting boron in the first transistor region and a portion of the second transistor region.

Amend claim 13 as follows:

13. (Amended) The method of claim 12, wherein implanting boron in the first transistor region and a portion of the second transistor region comprises the steps of:

performing a boron threshold adjustment implantation in the first transistor region and a portion of the second transistor region using a dose of about 3 E12 cm^{-2} and an energy of about 20 keV; and

performing a boron punch-through implantation in the first transistor region and a portion of the second transistor region using a dose of about 4 E12 cm^{-2} and an energy of about 70 keV.

Amend claim 16 as follows:

16. (Amended) The method of claim 1, wherein the first transistor device comprises a PMOS transistor, wherein the second transistor device comprises an NMOS transistor, and wherein implanting the first transistor region and a portion of the second transistor region using the first implantation process comprises implanting phosphorus in the first transistor region and a portion of the second transistor region.

Amend claim 17 as follows:

17. (Amended) The method of claim 16, wherein implanting phosphorus in the first transistor region and a portion of the second transistor region comprises the steps of:

performing a phosphorus threshold adjustment implantation in the first transistor region and a portion of the second transistor region using a dose of about 8 E11 cm^{-2} and an energy of about 20 keV; and

performing a phosphorus punch-through implantation in the first transistor region and a portion of the second transistor region using a dose of about 4 E12 cm^{-2} and an energy of about 70 keV.

Amend claim 18 as follows:

18. (Amended) A method of fabricating MOSFET transistors in a semiconductor device, comprising the steps of:

providing a semiconductor device substrate;

adjusting a threshold voltage of a first transistor device in a first region of said semiconductor device substrate; [using a first threshold adjust implantation process;] and concurrently forming a source/drain region of a second transistor device, both using the same implant [using the first threshold adjust implantation process].

Amend claim 19 as follows:

19. (Amended) The method of claim 18, further comprising the step of forming a source/drain region of the first transistor device [using a first LDD implantation process].

Amend claim 20 as follows:

20. (Amended) The method of claim 19, further comprising the steps of:

then forming a first gate oxide structure of the first transistor device having a first thickness; and

forming a second gate oxide structure of the second transistor device having a second thickness, the second thickness being greater than the first thickness.

Amend claim 21 as follows:

21. (Amended) The method of claim 19, further comprising the steps of[:] then

[using a second threshold adjust implantation process;] and forming a source/drain region of a fourth transistor device [using the second threshold adjust implantation process]

Amend claim 22 as follows:

22. (Amended) The method of claim 21, further comprising the steps of forming a source/drain region of the third transistor device using a second LDD implantation process.

Amend claim 25 as follows:

25. (Amended) The method of claim 18, wherein the first transistor device comprises a PMOS transistor, wherein the second transistor device comprises an NMOS transistor, and wherein adjusting a threshold voltage of the first transistor device and forming a source/drain region of the second transistor device [using the first threshold adjust implantation process] comprises selectively implanting a first transistor region associated with the first transistor device to adjust a threshold voltage associated with the first transistor device, and implanting a portion of a second transistor region associated with the second transistor device to form a source/drain region associated with the second transistor device using phosphorus.

Amend claim 26 as follows:

26. (Amended) A method of forming a source/drain region in a semiconductor device, comprising the steps of:

providing a semiconductor device substrate; and

selectively concurrently implanting a first transistor region in said semiconductor device substrate to adjust a threshold voltage associated with a first transistor device and a portion of a second transistor region to form a source/drain region associated with a second transistor device [using a single implantation process].

Amend claim 27 as follows:

27. (Amended) The method of claim 26, wherein selectively implanting the first transistor region and a portion of the second transistor region comprises the step of implanting one of phosphorus, arsenic and boron in the first transistor region and a portion of the second transistor region.

Amend claim 28 as follows:

28. (Amended) A method of fabricating a semiconductor device, comprising the steps of:

providing a semiconductor device substrate;

concurrently implanting in said semiconductor device substrate an active region of a low voltage NMOS device and source/drain regions of a high voltage PMOS device using a boron threshold voltage adjust implantation [process];

then concurrently implanting in said semiconductor device substrate an active region of a low voltage PMOS device and source/drain regions of a high voltage NMOS device using a phosphorus threshold voltage adjust implantation [process];

forming polysilicon gate structures associated with the high and low voltage

implanting source/drain regions associated with the low voltage NMOS device using a phosphorus or arsenic LDD implantation [process]; and

implanting source/drain regions associated with the low voltage PMOS device using a boron LDD implantation [process].